ENGT 050: DIGITAL LOGIC ANALYSIS

Originator
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Justification / Rationale
Labor market indicators show that there are jobs available and an advisory committee recommends the course.

Effective Term
Fall 2019

Credit Status
Credit - Degree Applicable

Subject
ENGT - Engineering Technology

Course Number
050

Full Course Title
Digital Logic Analysis

Short Title
DIGITAL LOGIC ANALYSIS

Discipline

Disciplines List
Engineering Technology

Modality
Face-to-Face

Catalog Description
This course covers combinational logic utilizing Boolean algebra and the binary numbering system. Topics include Karnaugh maps, truth tables, coding, switching circuits, converters, logic circuit elements, timers, digital-to-analog and analog-to-digital conversions, decoders, multiplexers, demultiplexers, and displays.

Schedule Description
This course covers combinational logic utilizing Boolean algebra and the binary numbering systems.
Advisory: MATH 060 or ESYS 004

Lecture Units
2
Lecture Semester Hours
36

Lab Units
1
Lab Semester Hours
54

In-class Hours
90

Out-of-class Hours
72

Total Course Units
3

Total Semester Hours
162

Prerequisite Course(s)
Advisory: MATH 060 or ESYS 004

Required Text and Other Instructional Materials

Resource Type
Book

Author
Floyd, Thomas L.

Title
Digital Fundamentals

Edition
11th

Publisher
Pearson

Year
2014

College Level
Yes

ISBN #
978-0132737968

Resource Type
Manual

Author
Floyd, Thomas L., Buchla, David

Title
Lab Manual for Digital Fundamentals

Publisher
Pearson

Year
2014

For Text greater than five years old, list rationale:
ISBN for lab manual: 978-0133514391

Class Size Maximum
30

Entrance Skills
Unit conversion skills

Prerequisite Course Objectives
ESYS 004-Convert units within the US and metric systems and between the US and metric system units using unit fractions.
MATH 060-Recognize and convert between units of measurements in the American and metric systems.
MATH 060-Use unit measure appropriately in applications.

Entrance Skills

Compute using four basic operations.

Prerequisite Course Objectives

ESYS 004-Compute using the four basic operations of addition, subtraction, multiplication, and division on the rational numbers.
ESYS 004-Apply the order of operations to simplify expressions involving several operations.
MATH 060-Apply the basic operations to solve application problems that involve whole numbers, integers, and rational numbers.
MATH 060-Apply the order of operations to simplify expressions involving several operations using rational numbers.

Entrance Skills

Math with fractions

Prerequisite Course Objectives

ESYS 004-Convert between improper fractions, mixed numbers, and decimals.
ESYS 004-Use the fundamental property of fractions and prime factorizations to write equivalent fractions.
MATH 060-Apply methods of conversion between percents, decimals, and fractions.

Entrance Skills

Perform math with variables.

Prerequisite Course Objectives

MATH 060-Understand the concept of a variable and how a variable can be used to represent an unknown quantity.
MATH 060-Evaluate an algebraic expression via substitution of rational numbers and determine if a given value is a solution to an algebraic equation

Course Content

1. Number systems and number system conversion
    a. Binary numbering system
    b. Octal numbering system
    c. Hexadecimal numbering system
    d. Binary Coded Decimal (BCD) system
    e. Binary addition
    f. Binary subtraction
2. Logic Gates
    a. Gate
    b. Inverters
    c. OR gate, AND gate, NAND gate, NOR gate
    d. Data control enable/inhibit
    e. AND gate enable/inhibit
    f. OR gate enable/inhibit
    g. NAND gate enable/inhibit
    h. NOR gate enable/inhibit
    i. Summary gate enable/inhibit
    j. NAND as an inverter
    k. NOR as an inverter
    l. Expanding an AND gate
    m. Expanding a NAND gate
    n. Expanding an OR gate
    o. Expanding a NOR gate
3. Waveforms and Boolean algebra
    a. Waveform analysis
    b. Delayed clock and shift-counter waveforms
    c. Combinational Logic
    d. Boolean theorems

   e. DeMorgan's Theorems
   f. Designing logic circuits
   g. AND-OR-INVERT gate
   h. Reducing Boolean expressions with Karnaugh maps
4. Exlusive-OR gate
   a. Enable/inhibit
   b. Waveform analysis
   c. Exclusive-NOR
   d. Exclusive-OR/NOR
   e. Parity
   f. Even-parity generator
   g. Even/odd-parity generator
   h. Parity checker
   i. Nine-bit parity generator/checker
   j. Comparator
5. Adders
   a. Half adder
   b. Full adder
   c. Ones complement adder/subtracter
   d. Twos complement adder/subtracter
   e. Binary-coded-decimal addition
   f. Binary-coded-decimal adder
6. Specifications and open-collector gate
   a. TTL subfamilies
   b. TTL electrical characteristics
   c. TTL supply currents
   d. TTL switching characteristics
   e. TTL open-collector gates
   f. Open-collector applications
   g. CMOS (Complementary Metal Oxide Semiconductor)
   h. CMOS subfamilies
   i. CMOS specifications
   j. Interfacing TTL (transistor-transistor logic) to CMOS
   k. Emitter Coupled Logic (ECL)
   l. Interfacing ECL to other logic families
   m. Surface mount technology
7. Flip-flops
   a. Introduction to flip-flops
   b. Crossed NAND set-reset flip-flops
   c. Crossed NOR set-reset flip-flops
   d. Comparisons
   e. Using a set-reset flip-flop as a debounce circuit
   f. The gated set-reset flip-flop
   g. The transparent D flip-flop
   h. The master-slave D flip-flop
   i. The pulse edge-triggered D flip-flop
8. Master-Slave D and JK flip-flops
   a. Toggling a master-slave D flip-flop
   b. The JK flip-flop
   c. The nonoverlapping clock
   d. The shift counter
   e. Asynchronous counter Design (Mod count)
   f. Synchronous counter Design (Mod count)
   g. Up/Down counter
   h. Typical JK ICs
9. Shift registers

   a. Shift register constructed from JK flip-flops
   b. Parallel and serial data
   c. Parallel-in serial-out
   d. Serial data transmission formats
   e. IC shift registers
   f. Serial data transmission formats
   g. IC shift registers
   h. Serial data standards
   i. The ASCII code
10. Schmitt-trigger inputs and clocks
   a. The Schmitt-trigger input
   b. Using a Schmitt-trigger to square-up an irregular wave
   c. Schmitt-trigger clock
   d. The 555 timer used as a clock
   e. Crystal oscillators
   f. One shot circuits and ICs
   g. The 555 used as a one shot Astable
11. Digital-to-Analog and Analog-to-Digital conversions
   a. Resistor networks for digital-to-analog conversion
   b. The TTL digital-to-analog converter
   c. Analog-to-digital conversion using voltage conversion
   d. The count-up and compare analog-to-digital converter
12. Decoders, multiplexers, demultiplexers and displays
   a. Decoders
   b. Demultiplexers
   c. Multiplexers
   d. Using a multiplexer to reproduce a desired truth table
   e. Multiplexer and demultiplexer
   f. The 8-trace scope multiplexer
   g. The Light Emitting Diode (LED)
   h. The 7-segment display
   i. The liquid crystal display

Lab Content

1. Troubleshooting a 4-bit adder using a 7483 integrated circuit
2. Determine the truth table from the following gates:
   a. Inverters
   b. OR gates
   c. AND gates
   d. NAND gates
   e. NOR gates
3. Data control enable/inhibit of the following gates
   a. AND gate
   b. OR gate
   c. NAND gate
   d. NOR gate
4. Waveforms and Boolean algebra
   a. From a combination logic circuit write a boolean expression and complete truth table
   b. From a truth table complete a truth table and construct a combination logic circuit
   c. Construct a decimal to BCD encoder using three OR gates
5. Determing the truth table from the following gates
   a. Exclusive-OR
   b. Exclusive-NOR
6. Data control enable/inhibit of the following gates
   a. Exclusive-OR
   b. Exclusive-NOR
7. Construct an even/odd-parity generator

8. Specifications and open-collector gates
    a. Measure 7404 TTL electrical characteristics
    b. Measure 74LS04 TTL electrical characteristics
9. Flip-flop characteristics and measurements
    a. The master-slave D flip-flop
    b. Construct a nonoverlapping clock Master-slave JK flip-flop
10. Shift registers
11. Digital-to-analog and analog-to-digital conversions lab construction
    a. Resistor networks for digital-to-analog conversion
    b. The TTL digital-to-analog converter
    c. Analog-to-digital conversion using voltage conversion
    d. The count-up and compare analog-to-digital converter
12. Construct a decimal up counter driver a 7 segment LED
13. Construct an asynchronous decade counter using JK flip-flops
14. Build a four-channel Multiplexer and Demultiplexer circuit

Course Objectives

	Objectives
Objective 1	Define decimal, binary, octal and hexadecimal numbering systems.
Objective 2	Recognize and distinguish different types of logic gates
Objective 3	Understand the function of logic gates
Objective 4	Determine the output of a digital logic circuit given inputs
Objective 5	Construct logic circuits and modify the circuit to given specifications

Student Learning Outcomes

	Upon satisfactory completion of this course, students will be able to:
Outcome 1	Compare and convert number systems from decimal to binary to octal to hexadecimal
Outcome 2	Recognize the schematics and use logic gates to arrive at a desired conclusion with any input
Outcome 3	Construct various logic circuits and modify circuits to specifications
Outcome 4	Analyze waveforms at various points in logic circuits

Methods of Instruction

Method	Please provide a description or examples of how each instructional method will be used in this course.
Discussion	Students will discuss the material during lecture and lab.
Laboratory	Laboratory will be used to gain a hands-on understanding of the material presented in lecture.
Lecture	Lecture will provide a theoretical introduction and explanation of the material being covered.
Participation	Students will be asked questions during lecture and lab.

Methods of Evaluation

Method	Please provide a description or examples of how each evaluation method will be used in this course.	Type of Assignment
Mid-term and final evaluations	Students will be tested through Canvas to determine their understanding of the material.	In Class Only
Group activity participation/observation	During lab students will work in teams to perform and solve the lab report. Students will discuss their findings with classmates.	In Class Only
Laboratory projects	Laboratory projects and findings will be evaluated to gain a better understanding for the students' comprehension of the material. During lab, students will perform the lab work. At home, students will write their lab report.	In and Out of Class

Student participation/contribution	Students will be evaluated by their participation in both lecture and lab.	In Class Only
Tests/Quizzes/Examinations	Quizzes and Exams will include multiple choice questions.	In Class Only
Written homework	Homework will be assigned via Canvas and some questions will require a short answer written response. Students will also be assigned lab reports to be completed at home.	Out of Class Only

Assignments

Other In-class Assignments

1. Take notes
2. Lab work
3. Lab notebook
4. Quizzes
5. Exams
6. Discussion

Other Out-of-class Assignments

1. Reading assignments
2. Writing assignments
3. Lab write-ups

Grade Methods

Letter Grade Only

Comparable Transfer Course Information

University System

CSU

Campus

CSU Long Beach

Course Number

ET 255

Course Title

Introduction to Digital Electronics

Catalog Year

2018

University System

CSU

Campus

California State Polytechnic University, Pomona

Course Number

ETE 230

Course Title

Introduction to Digital Logic

Catalog Year

2018

Rationale

Number systems and conversions, theory and practice of fundamental and universal gates,

MIS Course Data

CIP Code
15.0000 - Engineering Technology, General.

TOP Code
092400 - Engineering Technology, General

SAM Code
C - Clearly Occupational

Basic Skills Status
Not Basic Skills

Prior College Level
Not applicable

Cooperative Work Experience
Not a Coop Course

Course Classification Status
Credit Course

Approved Special Class
Not special class

Noncredit Category
Not Applicable, Credit Course

Funding Agency Category
Not Applicable

Program Status
Not program-applicable

Transfer Status
Transferable to CSU only

Allow Audit
No

Repeatability
No

Materials Fee
No

Additional Fees?
No

Files Uploaded

Attach relevant documents (example: Advisory Committee or Department Minutes)
EngrTech Advisory 02-27-18 Minutes and Handouts.pdf

Approvals

Curriculum Committee Approval Date
11/09/2018

Academic Senate Approval Date
11/29/2018

Board of Trustees Approval Date
12/14/2018

Chancellor's Office Approval Date
3/20/2019

Course Control Number
CCC000603621

Programs referencing this course
Engineering Technology AS Degree (http://catalog.collegeofthedesert.eduundefined?key=209)